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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/811,288	03/25/2004	Mark B. Rosenbluth	42P18620	2190

8791 7590 06/14/2006

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EXAMINER	
VERBRUGGE, KEVIN	

ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 06/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/811,288	ROSENBLUTH ET AL.	
	Examiner	Art Unit	
	Kevin Verbrugge	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/25/04, 1/19/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

The oath or declaration is defective. A new oath or declaration in compliance with 37 CFR 1.67(a) identifying this application by application number and filing date is required. See MPEP §§ 602.01 and 602.02.

The oath or declaration is defective because:

It does not state that the person making the oath or declaration believes the named inventor or inventors to be the original and first inventor or inventors of the subject matter which is claimed and for which a patent is sought.

The phrase "an original and joint inventor" should be replaced with the phrase "an original and first inventor."

Claim Objections

Claim 17 is objected to because of the following informalities: it depends on claim 19. Presumably it was intended to depend on claim 16 (that is how it was considered in this Office action). Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 2 recites the limitation "the digital logic network" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim 13 recites the limitation "the ternary tag value" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 7-12, 14-18, and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent 5,806,083 to Edgar.

Regarding claims 1, 2, 3, 7, 8, 9, 11, 12, 14, 15, 16, 17, and 18, Edgar shows the claimed content addressable memory as address recognition device 103 in Figs. 1, 2, 3, and 5.

More specifically, he shows the claimed at least one tag input as the input on bus 104 in Fig. 3, for example.

He shows the claimed at least one RAM as the RAMs 320 in Figs. 3 and 4.

Finally, he shows the claimed circuitry as logic device 324 in Figs. 3 and 4.

Regarding claim 10, Edgar shows the claimed operation in Fig. 5.

Regarding claim 20, Edgar shows computer network 100 in Fig. 1 which includes the claimed network components, all of which are standard network features. The claimed circuitry including the CAM is discussed in the rejection of other claims above.

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Claims 1, 2, 7-9, and 11-19 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent 5,450,351 to Heddes.

Regarding claims 1, 2, 7, 8, 9, 11, 12, 14, 15, 16, 17, and 18, Heddes shows the claimed CAM in Fig. 2, for example.

More specifically, Heddes shows the claimed tag input at the top of Fig. 2.

He shows the claimed at least one RAM as the three RAMs of Fig. 2.

He shows the claimed circuitry as the AND circuitry in Fig. 2.

Regarding claims 13 and 19, Heddes discloses don't care bits at column 4, line 3 and following and at column 6, line 66 and following.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4, 5, 6, 13, 19, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,806,083 to Edgar.

Regarding claims 4, 5, and 6, Edgar does not disclose the entire structure of logic device 324. For instance, although he shows three AND gates in Fig. 4 and mentions that logic device includes 64 6-input AND gates (column 4, lines 51-52), he does not show the actual structure of the 6-input AND gates which are typically constructed of a tree of five 2-input AND gates. The actual circuitry used by a designer who is implementing Edgar's device is a matter of design choice and may include a tree of AND gates, an OR gate, and NOT logic, as claimed.

Regarding claims 13 and 19, Edgar does not disclose don't care bits, however don't care bits were well-known at the time of the invention and it would have been obvious to one of ordinary skill in the art at the time the invention was made to include don't care bits in Edgar's device to allow for the possibility of multiple values matching a single entry (since each don't care bit has two values).

Regarding claim 21, Edgar does not disclose a line card having a network processor with multiple multi-threaded engines integrated on a single die, however it would have been obvious to one of ordinary skill in the art at the time the invention was

made to include such a line card in Edgar's system for the attendant advantages it includes (higher performance, smaller size, lower heat generation, etc.).

****

Claims 3, 4, 5, 6, 10, 20, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,450,351 to Heddes.

Regarding claims 3, 4, 5, and 6, Heddes does not disclose the structure of the AND logic shown in Fig. 2. The actual circuitry used by a designer who is implementing Edgar's device is a matter of design choice and may include a tree of AND gates, an OR gate, and NOT logic, as claimed.

Regarding claim 10, Heddes does not teach applying the multiple read operations to the same RAM, but it would have been obvious to one of ordinary skill in the art at the time the invention was made to do so to reduce the number of devices required. Partitioning a single RAM into multiple sections and treating each section as one of the RAMs shown by Heddes would allow the designer to reduce the number of devices required and therefore potentially save power, heat, cost, etc.

Regarding claim 20, Heddes does not disclose the claimed network forwarding device having a switch fabric, line cards, network port, and circuitry to process packets,

but at column 2, lines 3-8, he teaches that CAMs are useful in networks where a packet of data includes an address which is used as the keyword for a CAM to produce an address to which the data are to be directed. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the CAM device of Heddes in a network system which would typically include the claimed network components not explicitly shown by Heddes.

Regarding claim 21, Heddes does not disclose a line card having a network processor with multiple multi-threaded engines integrated on a single die, however it would have been obvious to one of ordinary skill in the art at the time the invention was made to include such a line card in Heddes's system for the attendant advantages it includes (higher performance, smaller size, lower heat generation, etc.).

Conclusion

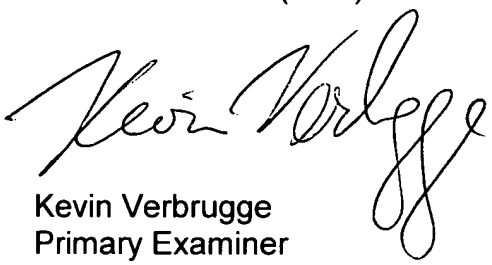
The method claims are grouped and rejected with the apparatus claims because the steps of the method are met by the disclosure of the apparatus and methods of the reference(s) as discussed above.

Any inquiry concerning this Office action should be directed to the Examiner by phone at (571) 272-4214.

Any response to this Office action should be labeled appropriately (including serial number, Art Unit 2189, and type of response) and mailed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, hand-carried or delivered to the

Customer Service Window at the Randolph Building, 401 Dulany Street, Alexandria, VA 22313, or faxed to (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197.



Kevin Verbrugge
Primary Examiner
Art Unit 2189